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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference S00P0920W000	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/JP 00/ 05783	International filing date (day/month/year) 28/08/2000	(Earliest) Priority Date (day/month/year) 30/08/1999
Applicant SONY CORPORATION et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.



It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

- a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.



the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

- b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :



contained in the international application in written form.



filed together with the international application in computer readable form.



furnished subsequently to this Authority in written form.



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the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.



the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. ☐ **Certain claims were found unsearchable** (See Box I).

3. ☐ **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

the text is approved as submitted by the applicant.



the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

the text is approved as submitted by the applicant.



the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No.

as suggested by the applicant.



because the applicant failed to suggest a figure.



because this figure better characterizes the invention.

1



None of the figures.

INTERNATIONAL SEARCH REPORT

national Application No

PCT/JP 00/05783

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 603 355 A (YAMADA HIDETOSHI ET AL) 29 July 1986 (1986-07-29)	6-13
A	claim 1; figures 2,6 ---	1-5
Y	GB 2 329 959 A (LG SEMICON CO LTD) 7 April 1999 (1999-04-07)	6-13
	figure 2 ---	
A	US 4 835 617 A (TODAKA YOSHIHIRO ET AL) 30 May 1989 (1989-05-30)	1-5
	figure 3 ---	
A	US 4 974 093 A (MURAYAMA JIN ET AL) 27 November 1990 (1990-11-27)	1-13
	column 3, line 25 - line 62 -----	

☐ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents :

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search

4 December 2000

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 4603355	A	29-07-1986	JP 1731439 C	29-01-1993
			JP 4017509 B	26-03-1992
			JP 59030376 A	17-02-1984
			DE 3329119 A	16-02-1984
<hr/>				
GB 2329959	A	07-04-1999	KR 246358 B	15-03-2000
			DE 19825048 A	08-04-1999
			JP 11164208 A	18-06-1999
<hr/>				
US 4835617	A	30-05-1989	JP 63078679 A	08-04-1988
			JP 63084275 A	14-04-1988
<hr/>				
US 4974093	A	27-11-1990	JP 1165270 A	29-06-1989
			JP 1176173 A	12-07-1989
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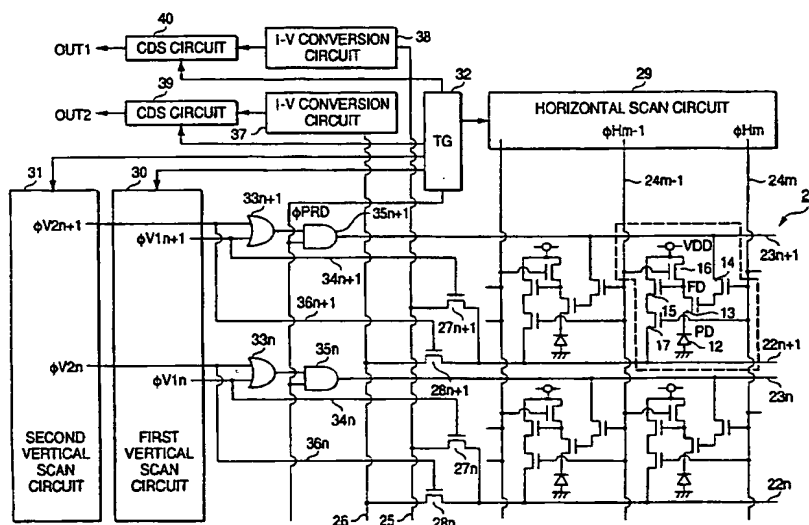
— *With international search report.*

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SOLID-STATE IMAGE PICKUP DEVICE, METHOD OF DRIVING THE SAME AND CAMERA SYSTEM



(57) **Abstract:** In a CMOS image pickup device in which the signal corresponding to the accumulated charge amount of each pixel is output to horizontal signal lines wired on a row basis, for example, two vertical selection transistors are provided every horizontal signal lines, and two vertical signal lines and two vertical scan circuits are provided every horizontal signal line, thereby separately outputting signals which are different in accumulation time and obtained by arbitrarily dividing 1 field into any number of parts on the basis of integer times of 1H.

WO 01/17234 A1

DESCRIPTION

SOLID-STATE IMAGE PICKUP DEVICE, METHOD OF DRIVING THE
SAME AND CAMERA SYSTEM

5

Technical Field

The present invention relates to a
solid-state image pickup device, a method of driving
the solid-state image pickup device and a camera
10 system, and particularly to an X-Y address type
solid-state image pickup device, a method of driving
the solid-state image pickup device, and a camera
system using the solid-state image pickup device as an
image pickup device.

15

Background Art

With an X-Y address type solid-state image
pickup device such as a CMOS image pickup device or the
like, an output signal which is substantially linearly
20 proportional to the amount of charges accumulated in
each unit pixel through photoelectric conversion is
obtained, and the dynamic range of the image pickup
device is determined by the amount of charges which can
be accumulated in each unit pixel.

25

Fig. 13 is an input/output characteristic
diagram showing the relationship between the light
amount of light incident to an image pickup device and

the output signal amount thereof. Apparent from the input/output characteristic diagram, the dynamic range of the image pickup device is determined by the saturated signal amount of each pixel and the noise level.

As described above, the charge amount which can be accumulated in the unit pixel is restricted due to the size of the pixel. Therefore, if the diaphragm of a camera lens is matched with a subject having low brightness in a camera system using this type of X-Y address type solid-state image pickup device as an image pickup device, the signal of a subject having high brightness is saturated. On the other hand, if the diaphragm of the camera lens is matched with a subject having high brightness, the signal of a subject having low brightness is embedded in noises, so that a broad dynamic range required for image recognition, etc. cannot be obtained.

Therefore, there has been proposed an X-Y address type solid-state image pickup device which can implement a broad dynamic range image pickup operation by outputting both of a long-time accumulated signal and a short-time accumulated signal during one field or one frame and obtaining an image pickup signal having contrast to an incident light amount in a very broad range on the basis of the long-time and short-time accumulated signals. Here, the long-time accumulated

signal is a signal based on signal charges which are accumulated for a long time, and the short-time accumulated signal is a signal based on signal charges which are accumulated for a short time.

5 In the conventional X-Y address type solid-state image pickup device, the long-time accumulated signal of one line is output and then the short-time accumulate signal of one line is output. Therefore, a vertical read-out scan pulse rises up
10 during a horizontal picture period or a horizontal scan circuit carries out a scanning operation twice during one horizontal scan period, which leaks into a camera signal processing circuit and appears as a vertically-striped system noise in the vicinity of the
15 center portion of the screen.

 Further, the long-time accumulated signal and the short-time accumulated signal are output from a single output terminal through a common signal line during the same horizontal scanning period, and thus
20 the output signal frequency is increased substantially twice for an image pickup device which does not carry out the broad dynamic range image pickup operation. Therefore, the power consumption is increased and the SN ratio is deteriorated.

25

Disclosure of Invention

The present invention has been implemented in

view of the foregoing situation, and has an object to provide a solid-state image pickup device which can eliminate the vertically-striped system noise in principle and prevent increase of the power consumption and deterioration of the SN ratio, a method of driving the solid-state image pickup device and a camera system using the solid-state image pickup device.

According to the solid-state image pickup device of the present invention, horizontal signal lines of plural rows are wired on a row basis in a pixel portion where unit pixels are arranged in a matrix form, and plural vertical signal lines are wired commonly to these horizontal signal lines of plural rows. The solid-stage image pickup device of the present invention is equipped with multiple-system vertical driving means which select each pixel of the pixel portion on a row basis over plural different rows and successively outputting to plural vertical signal lines signals which are output from the respective pixels to horizontal signal lines of plural rows, and horizontal driving means for successively selecting the respective pixels of plural rows which are selected by the vertical driving means. Further, the camera system of the present invention uses the solid-state image pickup device thus constructed as an image pickup device.

There has been considered such a construction

that two vertical signal lines are provided and a dual system of vertical driving means is provided in connection with the two vertical signal lines. In this construction, signals of two different columns are
5 output through the two vertical signal lines at the same time. At this time, a long-time accumulated signal and a short-time accumulated signal are output as dual system signals at the same time by making the accumulation time of signal charges different between
10 the respective pixels of the different two lines. In a camera system using this solid-state image pickup device as an image pickup device, coincidence (simultaneity) processing is carried out to set the long-time accumulated signal and the short-time
15 accumulated signal to signals on the same line, and then operating processing is carried out to implement a broad dynamic range image pickup operation.

Brief Description of Drawings

20 Fig. 1 is a diagram showing the construction of a CMOS image pickup device according to an embodiment of the present invention;

Fig. 2 is a timing chart of a vertical scan operation;

25 Fig. 3 is a timing chart of a horizontal scan operation;

Fig. 4 is a schematic diagram showing the

vertical scan operation in a broad dynamic range operation;

Fig. 5 is a diagram showing the time variation of a pixel accumulated charge amount in the broad dynamic range operation;

Fig. 6 is a circuit diagram showing another construction of a unit pixel;

Fig. 7 is a block diagram showing an example of the construction of a camera system according to the present invention;

Fig. 8 is a diagram showing the time variation of the pixel accumulated charge amount when the vertical driving system is a triple system;

Fig. 9 is a block diagram showing the construction of a signal processing circuit when the vertical driving system is a triple system;

Fig. 10 is an input/output characteristic diagram showing the relationship between an incident light amount and an output signal amount when the vertical driving system is a triple system;

Fig. 11 is a timing chart of the vertical scan operation in a high-speed image pickup operation;

Fig. 12 is a schematic diagram showing the vertical scan operation in the high-speed image pickup operation; and

Fig. 13 is an input/output characteristic diagram showing the relationship between the incident

light amount and the output signal amount of the image pickup device.

Best Mode for Carrying Out the Invention

5 Preferred embodiments according to the present invention will be described in detail hereunder with reference to the accompanying drawings by using a case where the present invention is applied to an X-Y address type solid-state image pickup device, for
10 example, a CMOS image pickup device.

Fig. 1 is a diagram showing the construction of a CMOS image pickup device according to an embodiment of the present invention.

15 In Fig. 1, an area surrounded by a broken line indicates an unit pixel 11. The unit pixel 11 includes five NchMOS transistors of a read-out transistor 13, a read-out selection transistor 14, an amplifying transistor 15, a reset transistor 16 and an output selection transistor 17 for a photodiode (PD) 12
20 serving as a photoelectric conversion element. A plurality of unit pixels 11 as described above are arranged in a matrix form to form a pixel portion 21.

25 In this case, in order to simplify the drawings, the pixel portion 21 is illustrated as being constructed in a pixel structure having two columns ((m-1)-th column, m-th column) and two rows (n-th row, (n+1)-th row). In the pixel portion 21, horizontal

signal lines $22n+1$, $22n$ and read-out lines $23n+1$, $23n$ are wired on a row basis. Further, horizontal selection lines $24m-1$, $24m$ are wired on a column basis.

5 In the unit pixel 11 on m -th column and $(n+1)$ -th row, the photodiode 12 serves at both of a photoelectric conversion function and a charge accumulating function. That is, the photodiode 12 serves to photoelectrically convert incident light to a signal charge having the charge amount corresponding to the light amount of the incident light, and further
10 accumulate the signal charge thus converted. The photodiode 12 is designed in a diode-buried type sensor structure, for example, in an HAD (Hole Accumulated Diode) sensor structure in which a hole accumulated
15 layer formed of $p+$ layer is added at the substrate surface side of an np diode.

The source of a read-out transistor 13 is connected to the cathode of the photodiode 12. The drain of the read-out transistor 13 is connected to a floated diffusion area FD serving as an accumulating
20 portion, and the gate thereof is connected to the source/drain of a read-out selection transistor 14. In the read-out selection transistor 14, the drain/source thereof is connected to a read-out line $23n+1$, and the
25 gate thereof is connected a horizontal selection line $24m$. In an amplifying transistor 15, the gate thereof is connected to the floated diffusion area FD, and the

drain thereof is connected to a power source VDD.

In a reset transistor 16, the source thereof is connected to the floated diffusion area FD, the drain thereof is connected to the power source VDD, and the gate thereof is connected to the adjacent horizontal signal line $24m-1$ of $(m-1)$ -th column. The reset transistor 16 is designed as a depression type to reset the floated diffusion area FD to the power source VDD. In an output selection transistor 17, the drain thereof is connected to the source of the amplifying transistor 15, the source thereof is connected to a horizontal signal line $22n+1$, and the gate thereof is connected to a horizontal selection line $24m$.

In connection with horizontal signal lines of plural rows (in this case, the horizontal signal lines $22n$, $22n+1$ of two rows), first and second vertical signal lines 25, 26 are wired in an area out of the pixel portion 21 so as to be perpendicular to the horizontal signal lines $22n$, $22n+1$. Vertical selection transistors $27n$, $27n+1$ and $28n$, $28n+1$ are connected between each of the horizontal signal lines $22n$, $22n+1$ and the first, second vertical signal lines 25, 26. These vertical selection transistors $27n$, $27n+1$, $28n$, $28n+1$ are also formed of NchMOS transistors.

On the peripheral portion of the pixel portion 21 are provided a horizontal scan circuit 29 for column selection as a horizontal driving system,

and both of a first vertical scan circuit 30 for row selection and a second vertical scan circuit 31 for controlling the accumulation time which serve as a vertical driving system. These scan circuits 29, 30 and 31 are formed of shift transistors, for example, and start a shift operation (scan) in response to a driving pulse given from a timing generator (TG) 32.

Horizontal scan (selection) pulses ϕ_{Hm-1} , ϕ_{Hm} are successively output from the horizontal scan circuit 29. These horizontal scan pulses ϕ_{Hm-1} , ϕ_{Hm} are supplied through the horizontal selection lines 24m-1, 24m to each gate of the read-out selection transistor 14, the reset transistor 16 and the output selection transistor 17 of the unit pixel 11 on a column basis. First vertical scan pulses ϕ_{V1n} , ϕ_{V1n+1} are successively output from the first vertical scan circuit 30, and second vertical scan pulses ϕ_{V2n} , ϕ_{V2n+1} are successively output from the second vertical scan circuit 31.

The first vertical scan pulses ϕ_{V1n} , ϕ_{V1n+1} are input to one of OR gates 33n, 33n+1 every row, and also supplied to the gates of the vertical selection transistors 27n, 27n+1 through the vertical selection lines 34n, 34n+1. The second vertical scan pulses ϕ_{V2n} , ϕ_{V2n+1} are input to the other of the OR gates 33n, 33n+1 every row, and supplied to the gates of the vertical selection transistors 28n, 28n+1 through the

vertical selection lines $36n$, $36n+1$.

The respective outputs of the OR gates $33n$, $33n+1$ are input to respective one input terminals of AND gates $35n$, $35n+1$, and a read-out pulse ϕ_{PRD} output from the timing generator 32 is input to the other input terminals of the AND gates $35n$, $35n+1$. Each output of the AND gates $35n$, $35n+1$ is supplied through the read-out line $23n$, $23n+1$ to the drain of the read-out selection transistor 14 in each pixel.

I(current)-V(voltage) conversion circuits 37, 38 for converting signal current to signal voltage and correlated double sampling circuits (hereinafter referred to as CDS) 39, 40 as differential circuits are provided at the output end sides of the first and second vertical signal lines 25, 26. The I-V conversion circuits 37, 38 convert to a signal voltage a pixel signal which is supplied as signal current through the vertical signal lines 25, 26 and then supply the signal voltage to CDS circuits 39, 40.

The CDS circuits 39, 40 perform processing of taking the difference between the noise level and the signal level just after pixel reset on the basis of the sampling pulse supplied from the timing generator 32. If necessary, an AGC (Auto Gain Control) circuit, an ADC (Analog Digital Converter) circuit, etc. may be provided at the subsequent stage of each of the CDS circuits 39, 40.

Next, the broad dynamic range operation in the CMOS image pickup device according to the embodiment of the present invention will be described with reference to the timing charts of Figs. 2 and 3.

5 Fig. 2 is a timing chart of the vertical scan operation, and Fig. 3 is a timing chart of the horizontal scan operation.

10 The first vertical scan pulse ϕV_{1n} and the second vertical scan pulse ϕV_{2n+i} are output from the first vertical scan circuit 30 and the second vertical scan circuit 31 respectively at a time t_1 by the vertical scan operation of the first and second vertical scan circuits 30, 31. The first vertical scan pulse ϕV_{1n} is applied through the vertical selection
15 line 34n to the gate of the vertical selection transistor 27n on the n-th row, and the second vertical scan pulse ϕV_{2n+i} is applied through the vertical selection line 36n+i to the gate of the vertical selection transistor 28n+i on the (n+i)-th row. As a
20 result, the n-th row, the (n+1)-th row are selected.

Under this state, the horizontal scan operation is carried out by the horizontal scan circuit 29. The horizontal scan operation will be described by paying attention to the m-th column, for example.

25 First, when the horizontal scan pulse ϕH_{m-1} is output from the horizontal scan circuit 29 and applied to a horizontal selection line 24m-1 on the

(m-1)-th column, the reset transistor 16 of the pixel of the m-th column is set to ON state, whereby the floated diffusion area FD is reset to the power source VDD through the reset transistor 16.

5 Subsequently, when the horizontal scan pulse ϕ_{Hm} is output from the horizontal scan circuit 29 and applied to the horizontal selection line 24m of the m-th column, the output selection transistor 17 of the pixel on the m-th column is set to ON state, whereby
10 the current corresponding to the reset level of the pixel (m,n) on the vertically selected n-th row and the horizontally selected m-th column is output through the horizontal signal line 22n and the vertical selection transistor 27n to the first vertical signal line 25,
15 and at the same time the current corresponding to the reset level of the pixel (m,n+i) on the vertically selected (n+i)-th row and the horizontally selected m-th column is output to the second vertical signal line 26 through the horizontal signal line 22n+i and
20 the vertical selection transistor 28n+i.

 When the read-out pulse ϕ_{PRD} is output during an occurrence period of the horizontal scan pulse ϕ_{Hm} , the logical product is taken between the read-out pulse ϕ_{PRD} and the first vertical scan pulse ϕ_{V1n} in the AND
25 gate 35n, and also between the read-out pulse ϕ_{PRD} and the second vertical scan pulse ϕ_{V2n+i} in the AND gate 35n+i. As a result, pulses rise up on the read-out

lines $23n$, $23n+i$ of the n -th and $(n+i)$ -th rows,
respectively. At this time, each of the read-out
selection transistors 14 at the pixels (m,n) , $(m,n+i)$
is set to ON state because the horizontal scan pulse
5 ϕ_{Hm} is applied to the gate thereof.

Accordingly, the read-out pulse ϕ_{PRD} applied
to the read-out lines $23n$, $23n+i$ is applied to the gate
of the read-out transistor 13 through the drain/source
of the read-out selection transistor 14 at the pixels
10 (m,n) , $(m,n+i)$, whereby the read-out transistor 13 is
set to ON state, and the signal charges which are
produced and accumulated through the photoelectric
conversion in the photodiode 12 are read out to the
floated diffusion area FD through the read-out
15 transistor 13.

When the read-out pulse ϕ_{PRD} is extinguished,
the read-out transistor 13 is set to OFF state. The
signal charges read into the floated diffusion area FD
are amplified in accordance with the charge amount
20 thereof by the amplifying transistor 15 and set to
signal current, and then output through the output
selection transistor 17 and then the horizontal signal
lines $22n$, $22n+i$ and the vertical selection transistors
 $27n$, $28n+i$ (as shown in Fig. 4) to the first and second
25 vertical signal lines 25, 26, respectively.

When the pixels (m,n) , $(m,n+i)$ are selected,
the pixels $(m+1, n)$, $(m+1, n+i)$ of the next column are

reset by the horizontal scan pulse ϕ_{Hm} . When the horizontal scan pulse ϕ_{Hm} is extinguished and the horizontal scan pulse ϕ_{Hm+1} is output from the horizontal scan circuit 29, the pixels $(m+1, n)$, $(m+1, n+i)$ on the next column are set to be selected.

By repeating the above series of operations, the reset level and the signal level of the unit pixels 11 of one line of the n -th row, and the reset level and the signal level of the unit pixels 11 of one line of the $(n+i)$ -th row are successively read out through the same passage (the horizontal signal line $22n$, the vertical selection transistor $27n$, $28n+i$ or the like) onto the first and second vertical signal lines 25, 26, respectively. These signal levels are converted from current to voltage in the I-V conversion circuits 37, 38, and then supplied to the CDS circuits 39, 40 to be subjected to noise cancel through correlated double sampling.

Subsequently, the second vertical scan pulse ϕ_{V2n} is output from the scan circuit 31 at a time t_2 through the vertical scan operation of the second vertical scan circuit 31. The second vertical scan pulse ϕ_{V2n} is applied to the gate of the vertical selection transistor $28n$ of the n -th row through the vertical selection line $36n$. As a result, the n -th row is selected. Each pixel on the n -th row is selected at the time t_1 by the vertical scan operation of the first

vertical scan circuit 30, and the photodiode 12 is reset.

Accordingly, the signal corresponding to the charge amount of charges which are photoelectrically converted and accumulated in the photodiode 12 for the accumulation time of $t_2 - t_1$ (that is, a long-time accumulation signal) at each pixel of the n -th row is output as an output OUT 2 through the horizontal signal line $22n$ of the n -th row and the vertical selection transistor $28n$ and the second vertical signal line 26. Since the signal is also read out from the photodiode 12 at this time point, the photodiode 12 is reset.

Again, the first vertical scan pulse ϕ_{V1n} is output from the scan circuit 30 at the time t_3 after one vertical scan period (1V) elapses from the time t_1 by the vertical scan operation of the first vertical scan circuit 30. The first vertical scan pulse ϕ_{V1n} is applied to the gate of the vertical selection transistor $27n$ of the n -th row through the vertical selection line $34n$. As a result, the n -th row is selected. Each pixel on the n -th row is selected at the time t_2 by the vertical scan operation of the second vertical scan circuit 31, and the photodiode 12 is reset.

Accordingly, in each pixel of the n -th row, the signal corresponding to the charge amount of charges which are photoelectrically converted and

accumulated for the accumulation time of $t_3 - t_2$ (that is, a short-time accumulation signal) in the photodiode 12 is output as an output OUT 1 through the horizontal signal line 22n of the n-th row \pm the vertical selection transistor 27n \pm the first vertical signal line 26.

Fig. 5 shows the time variation of the accumulated charge amount of a pixel in which the photodiode 12 is saturated in a normal read-out operation. In Fig. 5, a represents the signal level, b represents the saturation level, and c represents the white clip level. The saturation level b is dispersed among pixels.

A pixel which starts the charge accumulation at the time t_1 reaches the saturation level at the time t_2 , and the saturation level b is output as an output OUT2. At the time t_3 , the signal level a corresponding to the accumulation time of $t_3 - t_2$ is output as an output OUT1 from the pixel at the time t_3 . Here, if the timing is set so as to satisfy the condition: $(t_3 - t_2) \ll (t_2 - t_1)$, a pixel which is saturated at $(t_2 - t_1)$ is not saturated at $(t_3 - t_2)$.

Through a series of operations as described above, the long-time accumulation signal (saturation level b) and the short-time accumulation signal (signal level a) are output as the output OUT2 and the output OUT1 respectively from the same pixel with the time lag

of $(t_3 - t_2)$.

As described above, in the CMOS image pickup device in which the signal corresponding to the accumulation charge amount of each pixel is output to the horizontal signal lines $22n$, $22n+1$ arranged on a row basis, for example, two vertical selection transistors $27n$, $28n$, two vertical signal lines 25 , 26 and two vertical scan circuits 30 , 31 are arranged for each horizontal signal line, thereby outputting signals which are different in accumulation time and obtained by dividing 1 field into any number of parts with any integer times of $1H$ (H represents the horizontal scan period), that is, the long-time accumulation signal and the short-time accumulation signal.

Accordingly, the driving frequency of the CMOS image pickup device, that is, the signal output frequency can be set to the same as the image pickup device which does not carry out the broad dynamic range image pickup operation, so that increase of power consumption and deterioration of SN ratio can be prevented. In addition, no discontinuous timing pulse rises up during the horizontal picture period, and thus the vertically striped system noise can be prevented from occurring.

In this embodiment, the drain of the amplifying transistor 15 is connected to the power source VDD and the source thereof is connected through

the output selection transistor 17 to the horizontal signal line $22n+1$ in the unit pixel 11. However, as shown in Fig. 6, the unit pixel 11 may be designed in accordance with the construction of the I-V conversion circuits 37, 38 so that the drain of the amplifying transistor 15 is connected to the horizontal signal line $22n+1$ and the source thereof is connected through the output selection transistor 17 to GND.

The long-time accumulation signal and the short-time accumulation signal are output, and an image pickup signal having contrast to the incident light amount in a broad range is obtained on the basis of these signals. That is, in order to implement the broad dynamic range image pickup operation, the signals on the same row are used as the long-time accumulation signal and the short-time accumulation signal. On the other hand, the long-time accumulation signal and the short-time accumulation signal which are simultaneously output through the two vertical signal lines 25, 26 are signals on different rows.

With respect to the same row, as is apparent from the above description on the operation, the long-time accumulation signal is output at the time t_2 , and the short-time accumulation signal is output at the time t_3 . That is, there is a time difference of t_3-t_2 between the long-time accumulation signal and the short-time accumulation signal on the same row.

Accordingly, in order to implement the broad dynamic range image pickup operation, the long-time accumulation signal and the short-time accumulation signal on the same row are required to be made simultaneous with each other.

Fig. 7 shows an example of the construction of a camera system according to the present invention which is equipped with a signal processing system for satisfying the above requirement.

As is apparent from Fig. 7, the camera system according to the present invention comprises a CMOS image pickup device 41, an optical system containing a lens 42 and a signal processing circuit 43. In the camera system thus constructed, a CMOS image pickup device according to the above embodiment or a modification thereof is used as the CMOS image pickup device 41. The lens 42 focuses incident light (image light) from a subject (not shown) onto the imaging face of the CMOS image pickup device 41. On the basis of the image light focused on the imaging face, the CMOS image pickup device 41 outputs the short-time accumulation signal as the output OUT1 and the long-time accumulation signal as the output OUT2.

The signal processing circuit 43 comprises two white clip circuits 431, 432, a single delay circuit 433, two amplifiers 434, 435 and a single adder 436. In the signal processing circuit 43, the two white

clip circuits 431, 432 perform the processing of clipping the outputs OUT1, OUT2 of the CMOS image pickup device 41, that is, the short-time accumulation signal a and the long-time accumulation signal b by the white clip level (see Fig. 5) and making the dispersion of the saturation level of the respective pixels uniform.

The delay circuit 433 has a delay time of $t_3 - t_2$, and delays the long-time accumulation signal b to make the long-time accumulation signal b simultaneous with the short-time accumulation signal a. The amplifiers 434, 435 have gains G_1 , G_2 respectively, and amplify the short-time accumulation signal a and the long-time accumulation signal b respectively. The adder 436 adds the short-time accumulation signal a and the long-time accumulation signal b which are made simultaneous with each other and amplified, thereby obtaining a signal of $axG_1 + bxG_2$, that is, an image pickup signal having contrast to a broad-range incident light amount.

As described above, the CMOS image pickup device 41 which can output the short-time accumulation signal a and the long-time accumulation signal b separately from each other is used as the image pickup device. In addition, the short-time accumulation signal a and the long-time accumulation signal b on the same row which are output from the CMOS image pickup device

41 are made simultaneous with each other, and then processed, thereby implementing the broad dynamic range image pickup operation without inducing any vertically striped system noise.

5 Further, when the gain G2 of the amplifier 435 is set to zero in the signal processing circuit 43, only the short-time accumulation signal a is output as the image pickup signal, and thus an electronic shutter operation having an accumulation time of $t_3 - t_2$ is
10 carried out. That is, in the camera system according to the present invention which uses the CMOS image pickup device according to the above embodiment or modification thereof as the image pickup device, the broad dynamic range image pickup operation and the
15 electronic shutter operation can be selectively performed by switching the gain G2 of the amplifier 435.

 The CMOS image pickup device according to the above-described embodiment is designed so that the
20 vertical signal lines, the selection transistors and the vertical scan circuits of two systems are respectively provided, however, the number of systems in which the above parts are respectively provided is not limited to two. That is, the above parts may be
25 respectively provided in each of three or more systems. In this case, various input/output characteristics can be obtained by arbitrarily setting the ratio of

read-out timings t_1 : t_2 : t_3 :... at which signals are read out from the respective pixels, the delay amount of the delay circuit (delay time) and the gains of the operating units G_1 , G_2 , G_3 , ...

5 Here, there will be described such a case that the vertical signal lines, the vertical selection transistors and vertical scan circuits are provided for each of respective three systems. Fig. 8 shows the relationship between the accumulation time and the
10 accumulation charge amount of the pixel, and Fig. 9 shows the construction of a signal processing circuit 43' of a camera system in this case.

 The signal processing circuit 43' comprises three white clip circuits 441, 442, 443, two delay
15 circuits 444, 445, three amplifiers 446, 447, 448 and a single adder 449.

 In the signal processing circuit 43' thus constructed, the three white clip circuits 441, 442, 443 clip the outputs OUT_1 , OUT_2 , OUT_3 of the three
20 systems of the CMOS image pickup device, that is, the respective signals of the accumulation time (t_3-t_2) , (t_2-t_1) , t_1 by the white clip level (see Fig. 8) to make uniform the dispersion in the saturation level of the respective pixels.

25 The delay circuit 444 and the delay circuit 445 have a delay time of t_3-t_2 and a delay time of t_2-t_1 respectively, and delay the respective signals of

the accumulation time t_2-t_1 , t_1 , whereby the signals of the accumulation time t_2-t_1 , t_1 are made simultaneous with the signal of the accumulation time t_3-t_2 . The amplifiers 446, 447, 448 have gains G_1 , G_2 , G_3 , and
5 amplify the respective signals of the accumulation time t_3-t_2 , t_2-t_1 , t_1 . The adder 449 adds the respective signals which are made simultaneous with one another and amplified, thereby obtaining an image pickup signal having contrast to a broad-range incident light amount.

10 As an example, by setting the ratio of the read-out timing of the signal from each pixel to $t_1:t_2:t_3 = 4:6:7$ (accumulation time ratio 4:2:1) and setting the gains G_1 , G_2 and G_3 of the operating portion (amplifiers 446, 447, 448) to 0, 2 and -1
15 respectively, only a specific light amount portion can be picked up (that is, black clip + white clip). Fig. 10 shows an input/output characteristic at this time.

In the case of the CMOS image pickup device of the above-described embodiment, the high-speed image
20 pickup operation can be also supported by varying the driving timing. In the following description, an embodiment in which the high-speed image pickup operation can be supported will be described.

In the construction shown in Fig. 1, the
25 first vertical scan circuit 30 is put in charge of odd-number rows and the second vertical scan circuit 31 is put in charge of even-number rows as shown in the

timing chart of Fig. 11. That is, the vertical scan operation is carried out while skipping every other row so that the vertical scan pulses of the odd-number rows (... , ϕV_{1n} , ϕV_{1n+2} , ...) are output from the first vertical scan circuit 30, and the vertical scan pulses of the even-number rows (... , ϕV_{2n+1} , ϕV_{2n+3} , ...) are output from the second vertical scan circuit 31.

Accordingly, as shown in the schematic diagram of Fig. 12, signals of two rows can be simultaneously read out through the vertical selection transistors (... , $27n$, $27n+2$, ...), (... , $28n+1$, $28n+3$, ...) and the vertical signal lines 25, 26. As a result, the information of all the pixels can be picked up in half a time at the same operating frequency, thereby implementing the high-speed image pickup operation.

In this case, the high-speed image pickup operation of the CMOS image pickup device in which the vertical signal lines, the vertical selection transistors and the vertical scan circuits are provided for two systems is described. However, if the number of systems may be increased to three systems, four systems, etc., the information of all the pixels can be picked up in one-third time, one-fourth time, etc., and thus the higher-speed image pickup operation can be implemented.

In order to fabricate the CMOS image pickup device which can support only the high-speed image

pickup operation, if vertical start pulses of n are given to the vertical scan circuit to perform the vertical scan operation while skipping every $(n-1)$ rows, only one vertical scan circuit is sufficient although the vertical selection transistors and the vertical signal lines of n systems are provided.

The construction of the unit pixel according to the above embodiment and the modification is merely an example, and thus the present invention is not limited to the embodiment and the modification. That is, the present invention is applicable to general X-Y address type solid-stage image pickup devices in which each unit pixel has at least a photoelectric conversion element such as a photodiode or the like, a read-out transistor for reading out the accumulated charges thereof and a read-out selection transistor for selecting the read-out transistor.

As described above, according to the present invention, in the solid-state image pickup device designed so that the signal corresponding to the accumulated charge amount of each pixel is output to the horizontal signal lines wired on a row basis and the cameral system using the solid-state image pickup device as an image pickup device, plural vertical signal lines are provided in connection with each horizontal signal lines, and plural systems of vertical driving systems are disposed in connection with the

vertical signal lines, whereby plural signals which are different in accumulation time and obtained by dividing 1 field into any number of parts with any integer times of 1H can be separately output, so that the broad
5 dynamic range image pickup operation can be implemented without inducing any vertically striped system noise.

CLAIMS

1. A solid-state image pickup device comprising:
a pixel portion in which unit pixels are
5 arranged in a matrix form;

horizontal signal lines of plural rows
which are wired to said pixel portion on a row basis;
plural vertical signal lines which are
wired commonly to said horizontal signal lines of
10 plural rows;

vertical driving means of plural systems
which select the respective pixels of said pixel
portion every row over plural different rows, making
the accumulation time of signal charges of each pixel
15 of the plural selected rows different among the plural
rows, and successively outputting to said plural
vertical signal lines the signals which are output from
the respective pixels to said horizontal signal lines
of plural rows; and

20 horizontal driving means for
successively selecting the pixels of plural rows which
are selected by said plural systems of vertical driving
means.

2. The solid-state image pickup device as
25 claimed in claim 1, wherein said vertical driving means
of plural systems has vertical selection switches of
plural systems which are connected between each of said

horizontal signal lines of plural rows and said plural vertical signal lines, and plural vertical scan circuits which are provided in connection with said vertical selection switches of plural systems and successively drive said vertical selection switches of different rows by a vertical scan operation.

3. A method of driving a solid-state image pickup device comprising a pixel portion in which unit pixels are arranged in a matrix form, horizontal signal lines of plural rows which are wired to the pixel portion on a row basis, and plural vertical signal lines which are wired commonly to the horizontal signal lines of plural rows, characterized by the steps of:

selecting the respective pixels of the pixel portion every row over plural different rows; making the accumulation time of signal charges of each pixel of the plural selected rows different among the plural rows;

successively selecting the respective pixels of plural rows thus selected and outputting the signal of each pixel to the corresponding one of the horizontal signal lines of plural rows; and

outputting through the plural vertical signal lines the signals which are output from the respective pixels to the horizontal signal lines.

4. A camera system using as an image pickup device a solid-state image pickup device a solid-state

image pickup device comprising: a pixel portion in which unit pixels are arranged in a matrix form; horizontal signal lines of plural rows which are wired to said pixel portion on a row basis; plural vertical signal lines which are wired commonly to said horizontal signal lines of plural rows; vertical driving means of plural systems which select the respective pixels of said pixel portion every row over plural different rows, making the accumulation time of signal charges of each pixel of the plural selected rows different among the plural rows, and successively outputting to said plural systems of vertical driving means the signals which are output from the respective pixels to said horizontal signal lines of plural rows; and horizontal driving means for successively selecting the pixels of plural rows which are selected by said plural systems of vertical driving means.

5. The camera system as claimed in claim 4, further comprising a signal processing circuit containing delay means for making signals of plural different rows output from said solid-state image pickup device simultaneous with one another, and processing means for processing the signals of plural rows which are made simultaneous with one another by said delay means.

6. A solid-state image pickup device comprising: a pixel portion in which unit pixels are

arranged in a matrix form;

horizontal signal lines of plural rows which are wired to said pixel portion on a row basis;

5 a vertical line which is wired commonly to said horizontal signal lines of plural rows;

vertical driving means for selecting the pixels of said pixel portion wired to the respective row of said horizontal signal line; and

10 horizontal driving means for selecting the pixel of the row selected by said vertical driving means; wherein

said unit pixel comprises a photoelectric converter, a read-out transistor for reading out a signal charge, accumulated by said photoelectric
15 converter, into a storage unit, a read-out selection transistor for selecting the reading out of the signal charge by said read-out transistor, an amplifying transistor for converting the signal charge stored in said storage unit into an electrical signal and for
20 outputting the electrical signal as a pixel signal, a reset transistor for resetting the storage unit, and an output selection transistor for selecting the output of the pixel signal provided by said amplifying transistor.

25 7. A solid-state image pickup device as claimed in claim 1, wherein said vertical drive means successively output the pixel signals to said vertical

line via said horizontal signal line, said horizontal drive means feeds a horizontal selection pulse to said read out selection transistor and said output selection transistor.

5 8. A solid-state image pickup device as claimed in claim 7, wherein said horizontal selection pulse also serves as a reset pulse for an adjacent column of said unit pixel.

10 9. A solid-state image pickup device as claimed in claim 6, wherein said unit pixel outputs a reset level by said reset transistor during a reset operation and a signal level based on the signal charge photoelectrically converted by said photoelectric converter.

15 10. A solid-state image pickup device as claimed in claim 6, the device further comprises a circuit for determining a difference between the reset level and the signal level.

20 11. A solid-state image pickup device as claimed in claim 10, wherein said circuit is a correlated double sampling circuit.

25 12. A solid-state image pickup device as claimed in claim 6, the device further comprises means for outputting signals of different accumulation time periods.

13. A method for driving a solid-state image pickup device comprising

a pixel portion having a matrix of unit pixels, each unit pixel comprises a photoelectric converter, a read out transistor for reading out a signal charge, accumulated by said photoelectric converter, into a storage unit, a read out selection transistor for selecting the reading out of the signal charge by said read out transistor, an amplifying transistor for converting the signal charge stored in said storage unit into an electrical signal and for outputting the electrical signal as a pixel signal, a reset transistor for resetting said storage unit, and an output selection transistor for selecting the output of the pixel signal provided by said amplifying transistor,

horizontal signal lines of plural rows which are wired to said pixel portion on a row basis,

a vertical line which is wired commonly to said horizontal signal lines of plural rows,

vertical driving means for selecting the pixels of said pixel portion wired to the respective row of said horizontal signal line, and

horizontal driving means for selecting the pixel of the row selected by said vertical driving means, the method comprising the steps of:

resetting a storage unit by a reset transistor;

outputting a reset level of said reset transistor to a horizontal signal line through an

amplifying transistor;

reading out the signal charge of the
photoelectric converter into said storage unit;

outputting a signal level based on the signal
charge to said horizontal signal line through said
amplifying transistor; and

outputting the reset level and the signal
level to a vertical line through said horizontal signal
line sequentially.

FIG. 1

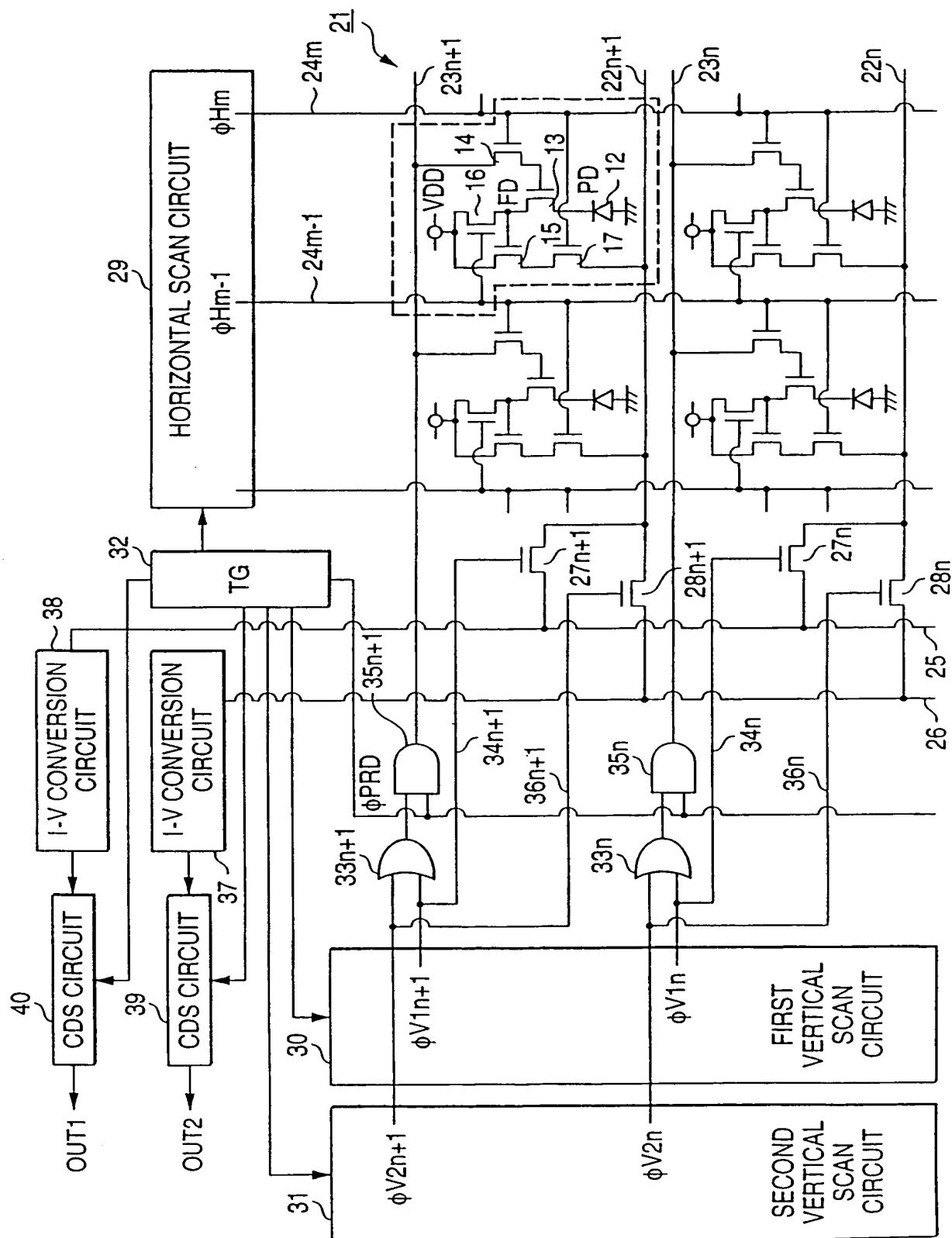


FIG. 2

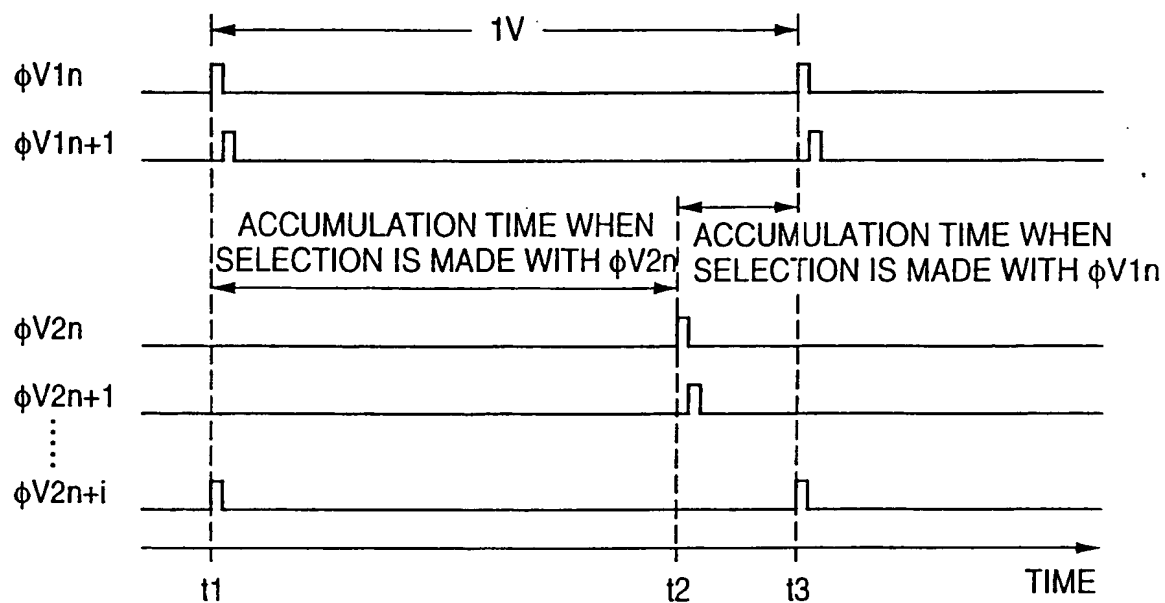
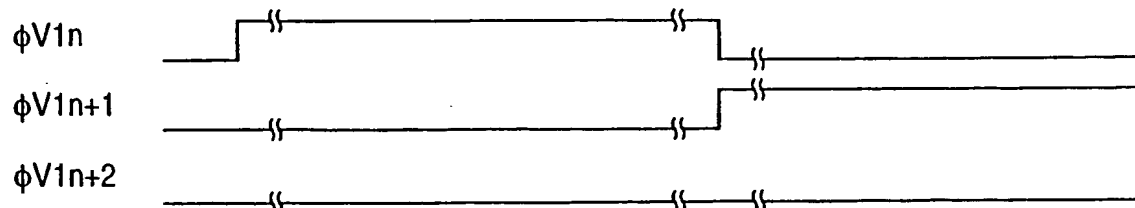
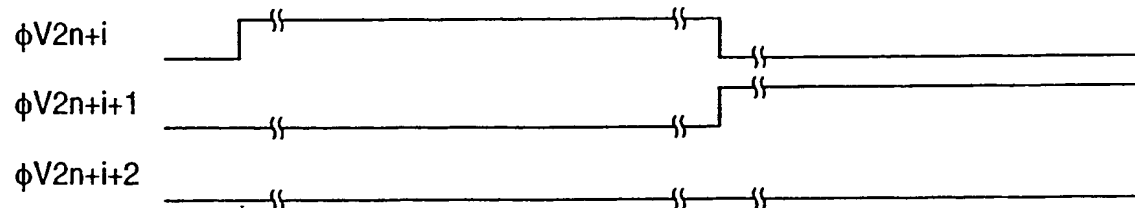


FIG. 3

FIRST VERTICAL SCAN PULSE



SECOND VERTICAL SCAN PULSE



READ-OUT PULSE



HORIZONTAL SCAN PULSE

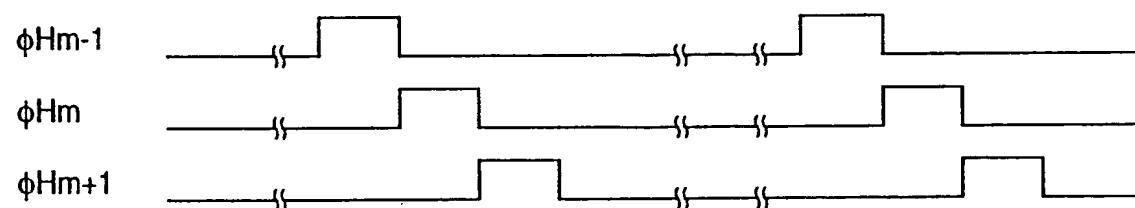
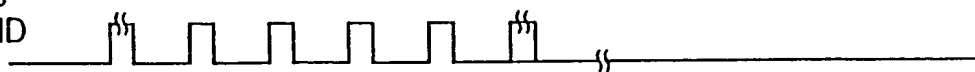
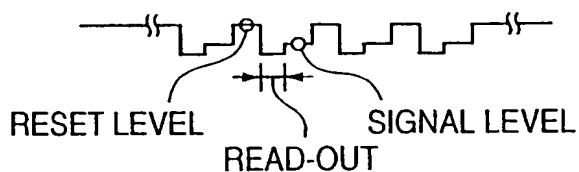
READ-OUT LINES
OF n -TH ROW AND
($n+i$)-TH ROWI-V
CONVERSION
OUT

FIG. 4

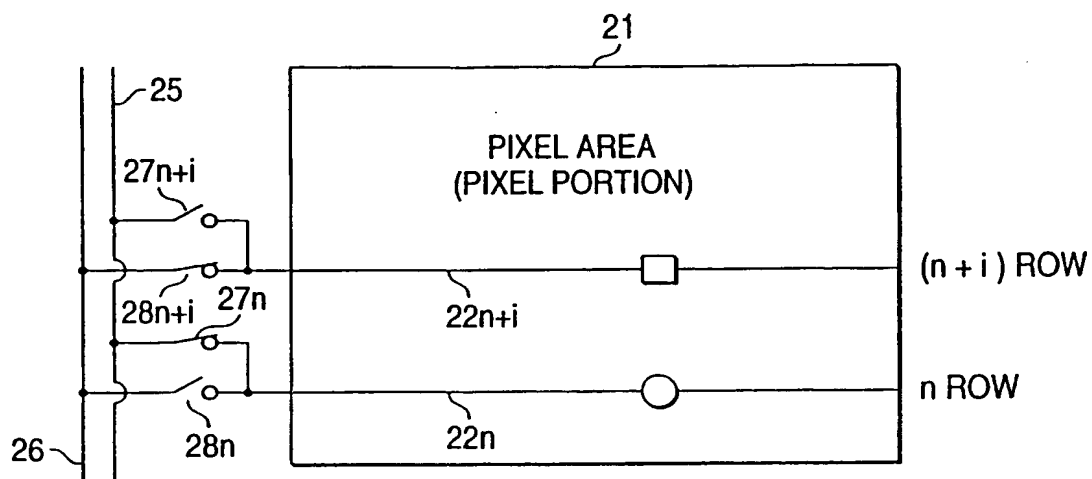


FIG. 5

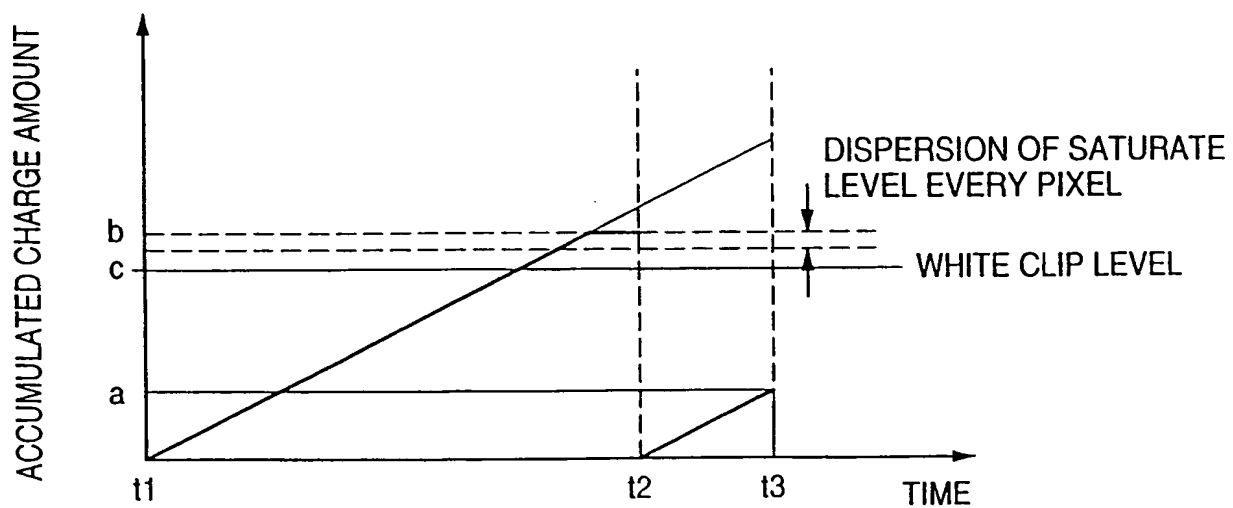


FIG. 6

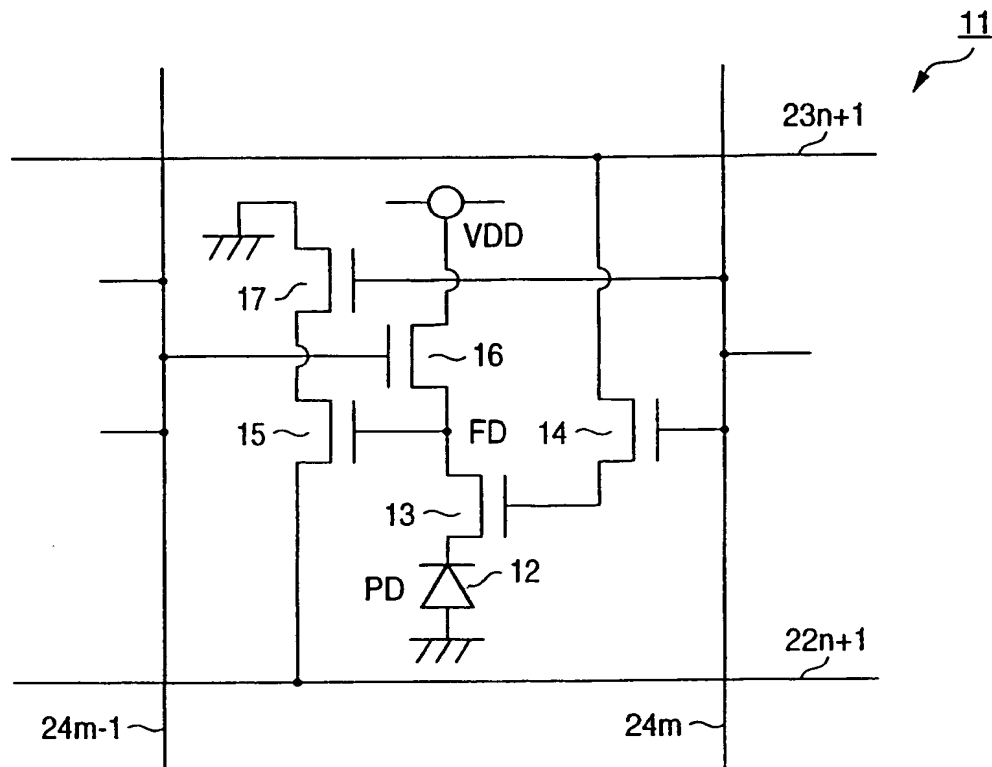


FIG. 7

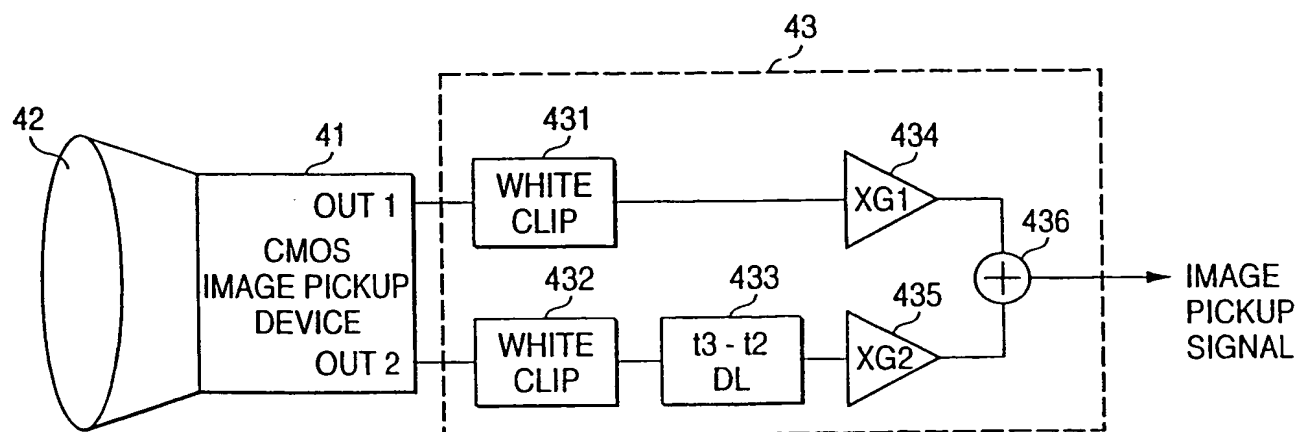


FIG. 8

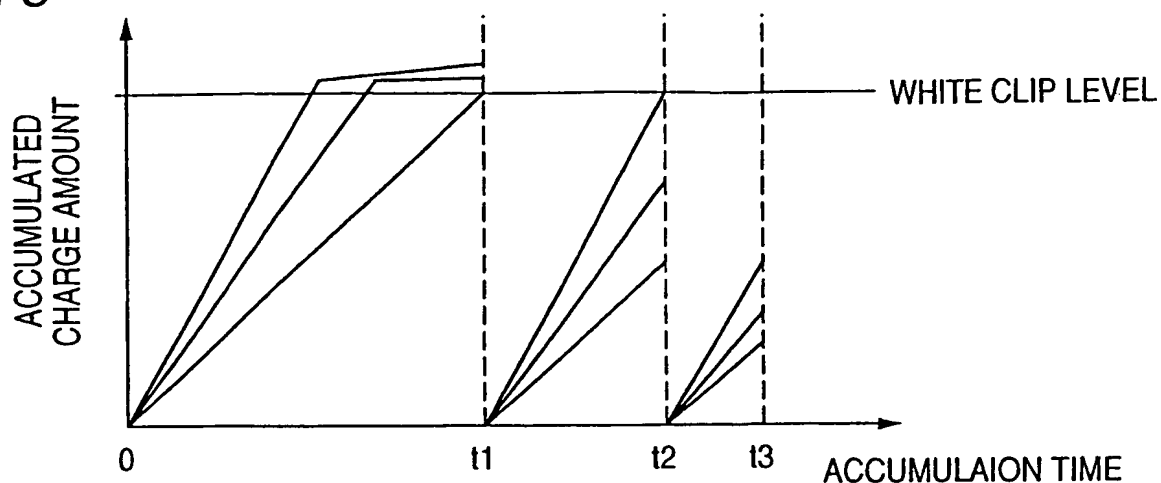


FIG. 9

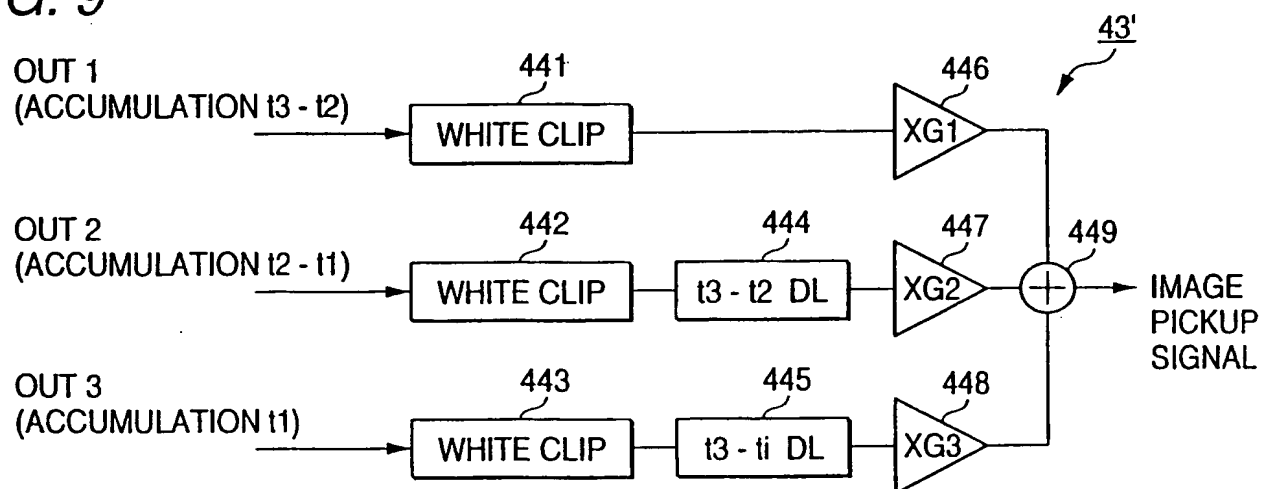


FIG. 10

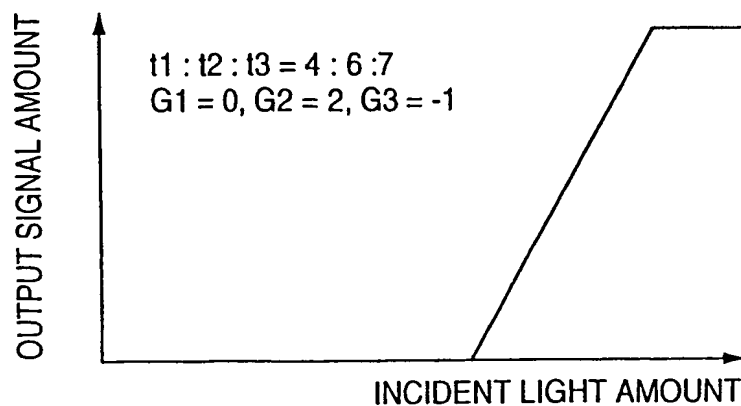


FIG. 11

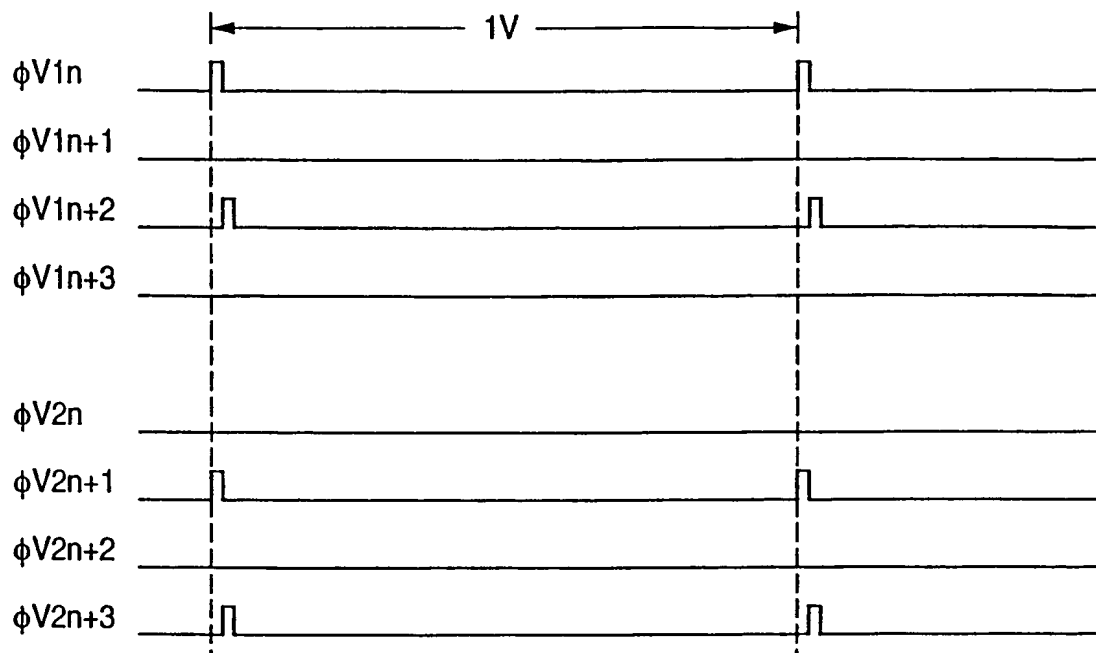


FIG. 12

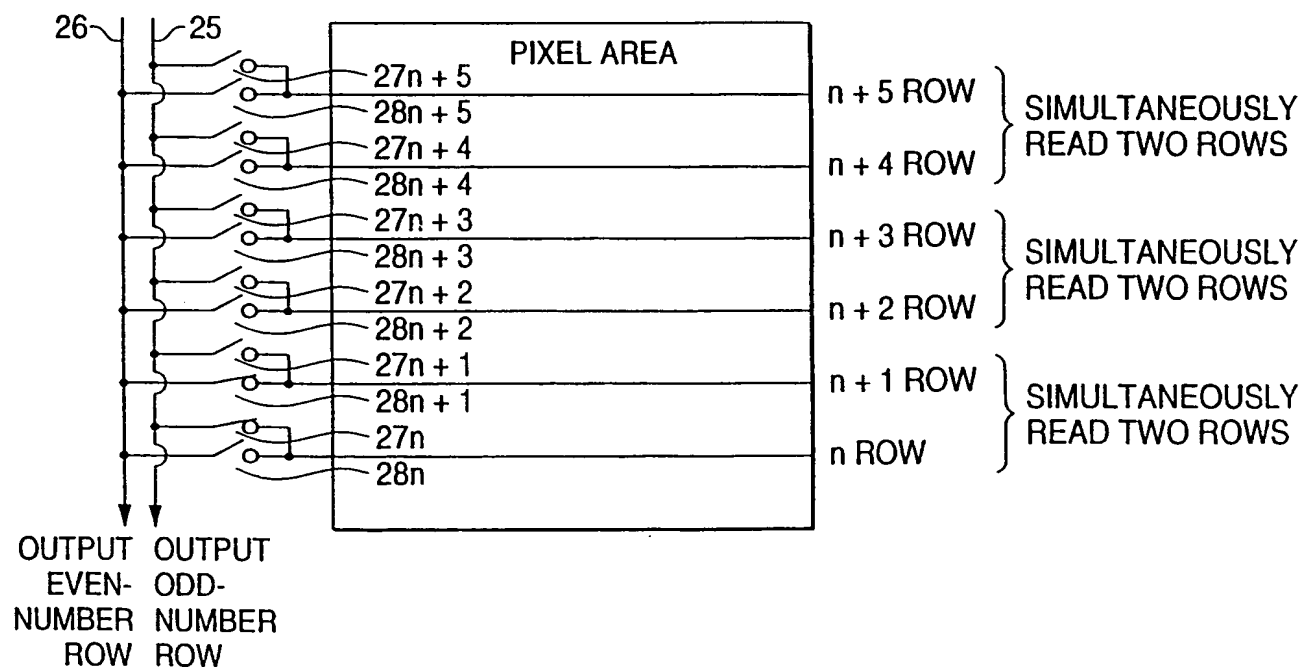
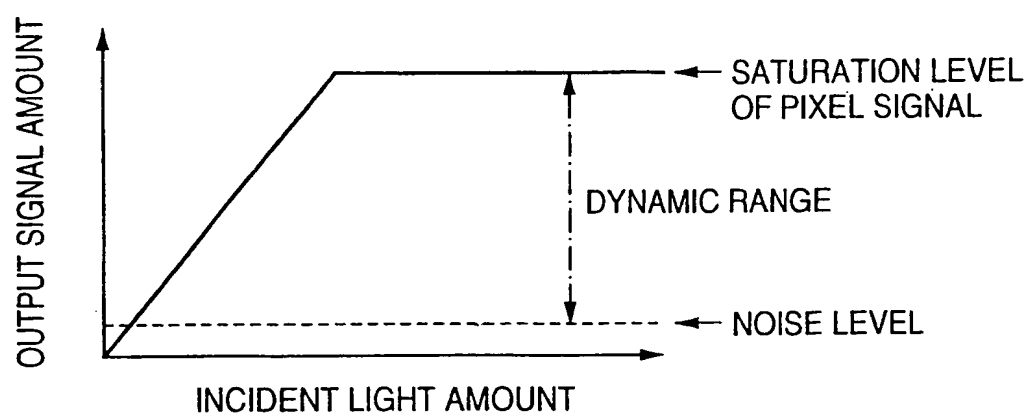


FIG. 13



DESCRIPTION OF REFERENCE NUMERALS

- 21 ... PIXEL AREA (PIXEL PORTION)
- 29 ... HORIZONTAL SCAN CIRCUIT
- 30 ... FIRST VERTICAL SCAN CIRCUIT
- 31 ... SECOND VERTICAL SCAN CIRCUIT
- 37, 38 ... I-V CONVERSION CIRCUIT
- 39, 40 ... CDS CIRCUIT
- 41 CMOS IMAGE PICKUP DEVICE

INTERNATIONAL SEARCH REPORT

Intern: al Application No

PCT/JP 00/05783

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04N3/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 603 355 A (YAMADA HIDETOSHI ET AL) 29 July 1986 (1986-07-29)	6-13
A	claim 1; figures 2,6 ---	1-5
Y	GB 2 329 959 A (LG SEMICON CO LTD) 7 April 1999 (1999-04-07)	6-13
	figure 2 ---	
A	US 4 835 617 A (TODAKA YOSHIHIRO ET AL) 30 May 1989 (1989-05-30)	1-5
	figure 3 ---	
A	US 4 974 093 A (MURAYAMA JIN ET AL) 27 November 1990 (1990-11-27)	1-13
	column 3, line 25 - line 62 -----	

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

* & * document member of the same patent family

Date of the actual completion of the international search

4 December 2000

Date of mailing of the international search report

12/12/2000

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Authorized officer

Montanari, M

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/JP 00/05783

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4603355 A	29-07-1986	JP 1731439 C	29-01-1993
		JP 4017509 B	26-03-1992
		JP 59030376 A	17-02-1984
		DE 3329119 A	16-02-1984
GB 2329959 A	07-04-1999	KR 246358 B	15-03-2000
		DE 19825048 A	08-04-1999
		JP 11164208 A	18-06-1999
US 4835617 A	30-05-1989	JP 63078679 A	08-04-1988
		JP 63084275 A	14-04-1988
US 4974093 A	27-11-1990	JP 1165270 A	29-06-1989
		JP 1176173 A	12-07-1989

REC'D 26 MAR 2001

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国際予備審査報告

(法第12条、法施行規則第56条)
〔PCT36条及びPCT規則70〕

9/830518

出願人又は代理人 の書類記号 E 5 4 8 7 - 0 0	今後の手続きについては、国際予備審査報告の送付通知（様式PCT/ IPEA/416）を参照すること。	
国際出願番号 PCT/J P 0 0 / 0 5 8 8 3	国際出願日 (日.月.年) 3 0 . 0 8 . 0 0	優先日 (日.月.年)
国際特許分類 (IPC) Int.Cl ⁷ C 0 8 L 7 1 / 1 2 , C 0 8 K 5 / 4 9 , B 3 2 B 1 5 / 0 8		
出願人 (氏名又は名称) 旭化成株式会社		

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- II ☐ 優先権
- III ☐ 新規性、進歩性又は産業上の利用可能性についての国際予備審査報告の不作成
- IV ☐ 発明の単一性の欠如
- V ☒ PCT35条(2)に規定する新規性、進歩性又は産業上の利用可能性についての見解、それを裏付けるための文献及び説明
- VI ☒ ある種の引用文献
- VII ☐ 国際出願の不備
- VIII ☐ 国際出願に対する意見

国際予備審査の請求書を受理した日 1 1 . 1 0 . 0 0	国際予備審査報告を作成した日 0 6 . 0 3 . 0 1		
名称及びあて先 日本国特許庁 (IPEA/J P) 郵便番号100-8915 東京都千代田区霞が関三丁目4番3号	特許庁審査官 (権限のある職員) 吉澤 英一	4 J	9 5 4 3
電話番号 03-3581-1101 内線 3493			

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- ☐ 請求の範囲 第 _____ 項、 出願時に提出されたもの
 請求の範囲 第 _____ 項、 PCT19条の規定に基づき補正されたもの
 請求の範囲 第 _____ 項、 国際予備審査の請求書と共に提出されたもの
 請求の範囲 第 _____ 項、 _____ 付の書簡と共に提出されたもの
- ☐ 図面 第 _____ ページ/図、 出願時に提出されたもの
 図面 第 _____ ページ/図、 国際予備審査の請求書と共に提出されたもの
 図面 第 _____ ページ/図、 _____ 付の書簡と共に提出されたもの
- ☐ 明細書の配列表の部分 第 _____ ページ、 出願時に提出されたもの
 明細書の配列表の部分 第 _____ ページ、 国際予備審査の請求書と共に提出されたもの
 明細書の配列表の部分 第 _____ ページ、 _____ 付の書簡と共に提出されたもの

2. 上記の出願書類の言語は、下記に示す場合を除くほか、この国際出願の言語である。

上記の書類は、下記の言語である _____ 語である。

- ☐ 国際調査のために提出されたPCT規則23.1(b)にいう翻訳文の言語
☐ PCT規則48.3(b)にいう国際公開の言語
☐ 国際予備審査のために提出されたPCT規則55.2または55.3にいう翻訳文の言語

3. この国際出願は、ヌクレオチド又はアミノ酸配列を含んでおり、次の配列表に基づき国際予備審査報告を行った。

- ☐ この国際出願に含まれる書面による配列表
☐ この国際出願と共に提出されたフレキシブルディスクによる配列表
☐ 出願後に、この国際予備審査(または調査)機関に提出された書面による配列表
☐ 出願後に、この国際予備審査(または調査)機関に提出されたフレキシブルディスクによる配列表
☐ 出願後に提出した書面による配列表が出願時における国際出願の開示の範囲を超える事項を含まない旨の陳述書の提出があった
☐ 書面による配列表に記載した配列とフレキシブルディスクによる配列表に記載した配列が同一である旨の陳述書の提出があった。

4. 補正により、下記の書類が削除された。

- ☐ 明細書 第 _____ ページ
☐ 請求の範囲 第 _____ 項
☐ 図面 図面の第 _____ ページ/図

5. ☐ この国際予備審査報告は、補充欄に示したように、補正が出願時における開示の範囲を越えてされたものと認められるので、その補正がされなかったものとして作成した。(PCT規則70.2(c) この補正を含む差し替え用紙は上記1.における判断の際に考慮しなければならず、本報告に添付する。)

V. 新規性、進歩性又は産業上の利用可能性についての法第12条（PCT35条(2)）に定める見解、それを裏付ける文献及び説明

1. 見解

新規性 (N)	請求の範囲	1-12	有
	請求の範囲		無
進歩性 (IS)	請求の範囲	1-12	有
	請求の範囲		無
産業上の利用可能性 (IA)	請求の範囲	1-12	有
	請求の範囲		無

2. 文献及び説明 (PCT規則70.7)

請求項1-12に記載された発明である硬化性樹脂組成物、硬化樹脂組成物、硬化性複合材料、積層体、及び、樹脂付き金属箔については、国際調査報告に示されたいずれの文献にも記載されておらず、また、当業者にとり自明なものでもない。

VI. ある種の引用文献

1. ある種の公表された文書 (PCT規則70.10)

出願番号
特許番号公知日
(日. 月. 年)出願日
(日. 月. 年)優先日 (有効な優先権の主張)
(日. 月. 年)

J P, 2 0 0 0 - 2 9 0 4 9 0, A
公知日 (1 7. 1 0. 0 0)
出願日 (0 1. 0 4. 9 9)
[E X] 特許請求の範囲及び【0 0 3 3】

2. 書面による開示以外の開示 (PCT規則70.9)

書面による開示以外の開示の種類

書面による開示以外の開示の日付
(日. 月. 年)書面による開示以外の開示に言及している
書面の日付 (日. 月. 年)